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Presented for filing is a new divisional patent application of:

Applicant: HONGYONG ZHANG

Title: METHOD OF FABRICATING SEMICONDUCTOR DEVICE

Enclosed are the following papers, including all those required to receive a filing date under 37 CFR §1.53:

	Pages
Specification	14
Claims	1
Abstract	1
Declaration	2 (copy from parent)
Drawing(s)	6

"EXPRESS MAIL" Mailing Label Number EL 339 805 974 US
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Mike Augustine
M.G. Augustine

Enclosures:

- Rule 63 declaration, copy from a previous application under rule 63(d) for continuation or divisional only.
- Information Disclosure Statement: Applicant calls attention to documents listed on attached form(s) PTO-892 and PTO-1449 from parent case(s). Per Rule 97(d) copies of those documents are not provided.
- Postcard.

This application is a divisional (and claims the benefit of priority under 35 USC §120) of U.S. application serial no. 08/753,428, filed November 25, 1996. The disclosure of the prior application is considered part of (and is incorporated by reference in) the disclosure of this application.

Preliminary Amendment:

Page 1 of the specification, before line 1, insert --This is a divisional of U.S. application serial no. 08/753,428, filed November 25, 1996, (pending).--

The prior application is assigned of record to Semiconductor Energy Laboratory Co., Ltd., a Japanese corporation, by virtue of an assignment submitted to the Patent and Trademark Office for recording on November 25, 1996, at Reel 8279, Frame 0140.

Priority is claimed under 35 USC §119 based on priority application serial number 7-332629, filed November 27, 1995, in Japan.

1 Total Claims, 1 independent:

Basic filing fee	$ 760.00
Total claims in excess of 20 times $18.00	0.00
Independent claims in excess of 3 times $78.00	0.00
Multiple dependent claims	0.00
Total filing fee:	$ 760.00

A check for the filing fee is enclosed. Please apply any other required fees or any credits to deposit account 06-1050, referencing the attorney docket number shown above.

If this application is found to be INCOMPLETE, or if a telephone conference would otherwise be helpful, please call the undersigned at 619/678-5070.

Kindly acknowledge receipt of this application by returning the enclosed postcard.

Please send all correspondence to:

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Respectfully submitted,

Scott C. Harris
Reg. No. 32,030

Enclosures

98189.LJ1

APPLICATION

FOR

UNITED STATES LETTERS PATENT

TITLE: METHOD OF FABRICATING SEMICONDUCTOR DEVICE

APPLICANT: HONGYONG ZHANG

"EXPRESS MAIL" Mailing Label Number EL 339 805 974 US
Date of Deposit July 28, 1999
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Mike Augustine
M. E. Augustine

METHOD OF FABRICATING SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

1.Field of the Invention

The present invention relates to a method of fabricating a semiconductor device, using a crystalline thin-film semiconductor and, more particularly, to a method of fabricating planar type thin-film transistors.

2. Description of Related Art

In recent years, techniques for fabricating thin-film transistors (TFTs) on cheap glass substrates have evolved rapidly, because there is an increasing demand for active matrix liquid crystal displays.

An active matrix liquid crystal display has millions of pixels arranged in rows and columns. TFTs are arranged at these pixels. Electric charge going in and out of each electrode at the pixels is controlled by the switching action of the TFTs.

Therefore, if one TFT fails to operate, then pixel electrodes connected with the faulty TFT do not act as display elements. This gives rise to a so-called point defect. For example, in the case of a normally black liquid crystal display, when white color is displayed, the point defect appears as a black point, which is deeply harmful to the appearance. Furthermore, it has been required that a circuit (known as a peripheral driver circuit) for driving TFTs for displaying these pixel electrodes be formed out of TFTs integrated with the former TFTs on the same glass substrate.

In this case, if one driving TFT fails to operate, all TFTs applied with a driving voltage from the faulty TFT do not act as switching elements. This results in a so-called line defect. This is a fatal hindrance to the liquid crystal display.

Accordingly, in an active matrix liquid crystal display, millions of TFTs must operate normally and stably over a long term. However, the present situation is that it is difficult to eliminate point defects and line defects perfectly . One of the causes is poor contact. Poor contact is that an interconnect electrode is poorly electrically connected with an associated TFT at a contact location, thus a defective operation is occurred. Especially, in the case of a planar TFT, poor contact presents serious problems, because an interconnect electrode is electrically connected with an associated TFT through a thin contact hole.

The poor contact is a main cause of premature deterioration of semiconductor device characteristics. Especially, where large currents flow or the device is operated at high temperatures, the deterioration coursed by the poor contact is promoted. Therefore, it is said that the reliability of contacts determines the reliability of the semiconductor device.

Generally, in the case of pixel display regions of an active matrix liquid crystal display, the gate electrodes are brought out of the pixel display regions directly and so no contacts exist. That is, contact with the pixel electrodes is very important for the reliability of the liquid crystal display.

In the case of a peripheral driver circuit, very many (from tens of thousands to millions) contacts exist. Especially, because there exist gate electrode contacts, and because the temperature is elevated by large-current operation, the contacts must have higher reliability than the pixel display regions.

SUMMARY OF THE INVENTION

The causes of poor contact are classified into three major categories.

The first category is that a conductive film forming interconnect

electrodes is not in ohmic contact with a semiconductor film forming the source/drain regions of TFTs. This is caused by formation of an insulating coating such as a metal oxide at the junction plane. Also, the states of the vicinities of the semiconductor film surface (doping concentration, defect level density, cleanliness, and so on) greatly affect the performance of the contacts.

The second category is that the conductive film forming the interconnect electrodes has poor coverage and thus the interconnect line breaks within a contact hole. In this case, it is necessary to improve the situation by the method of forming the interconnect electrodes or changing the film growth conditions better.

The third category is that an interconnect electrode breaks due to the cross-sectional shape of the contact hole. The cross-sectional shape of the contact hole depends heavily on the conditions under which the insulators (SiN, SiO_2, etc.) covered with the contact portions are etched.

In order to form contacts with good coverage, it is desired to have a continuously mildly changing cross-sectional shape, or a tapering shape. Overetch of the underlying films (wedge-shape recess) which is often encountered with insulating films between plural layers severely deteriorates the coverage.

It is an object of the present invention to provide a semiconductor device having contact holes through which interconnect electrodes are electrically connected with TFTs, the device being characterized in that the contact holes have improved cross-sectional shape, whereby reducing malfunctions of the TFTs which would normally be caused by poor contact.

It is a more specific object of the invention to provide a liquid crystal display having contacts of improved reliability, whereby the liquid crystal display has improved long-term reliability.

It is another object of the invention to provide a method of fabricating semiconductor devices with an improved yield by eliminating point defects and line defects.

One aspect of the invention lies in a method of fabricating a thin-film transistor comprising a gate region having a gate electrode made of a material capable of being anodized and source/drain regions made of a semiconductor. This method comprises the steps of: forming a multilayer insulating film comprises at least two layers which have a common constituent over said gate region and over said source/drain regions; and forming holes in said multilayer insulating film by dry etching techniques so as to form tapered sections having tilt angles which decrease successively from said top insulating layer toward said bottom insulating layer.

In one feature of the invention, the dry etch rates of the interlayer insulating films are controlled so as to form tapered sections. As a result, the tilt angles of the cross-sectional shape of the contact holes decrease successively from the top layer toward the bottom layer. The tilt angles of the bottom layer and the top layer are indicated by α and ß, respectively, in Fig. 3.

It is only necessary that the insulating films act only as interlayer insulating films and so they can be made from various materials such as silicon oxide, silicon nitride, and organic resins.

Preferably, the used material permits easy control of the dry etch rates, because desired taper can be readily accomplished by making the etch rate of the upper layer higher than that of the lower layer.

Generally, where contact holes are formed by dry etching techniques, reactive ion etching (RIE) is used. However, RIE has the disadvantage that if the instant (known as endpoint) at which the etching process ends is not clear, then a conductive thin film to which

contact should be made is also etched away.

In the case of RIE, it is conventional to detect light emission due to a plasma in order to detect the endpoint. Specifically, certain radicals or ions produced during etching are monitored.

In this case, an interlayer insulating film consisting of silicon oxide which is formed on a gate-insulating film made of silicon oxide, for example, is etched. Light-emitting species to be monitored are mixed. This makes it difficult to confirm the endpoint.

Where the foregoing is taken into consideration, it is necessary that a insulating film used as an interlayer insulating film be selected, taking full account of the structure of the fabricated TFTs.

Another aspect of the invention lies in a method of fabricating a thin-film transistor comprising a gate region having a gate electrode made of a material capable of being anodized and source/drain regions made of a semiconductor. This method comprises the steps of: forming a thin film; forming a insulating film having a bottom surface over said gate region and over said source/drain regions such that said thin film is in contact with the bottom surface of said insulating film; forming holes in said insulating film by dry etching techniques; etching said thin film in contact with the bottom surface of said insulating film; and subjecting said holes to a light etching process.

In another feature of the invention, the contact holes are widened by the light etching process. Tapered section are formed around the tops of the contact holes.

If the thin film in contact with the bottom surface of the insulating film is etched by dry etching techniques, the insulating film is undercut because of isotropic etching. Hence, holes are formed. The undercutting will give rise to overetch, which in turn permits the interconnect electrodes to break later.

In the present invention, the light etching process can widen the contact holes by removing the undercutting inside the contact holes.

The light etching process is carried out with a higher O_2 content than during the step of forming the contact holes.

This eliminates overetch and, at the same time, causes resist mask for forming the contact holes to be recessed. The corners at the edges (the outer frames around the entrances to the contact holes) are rounded off.

That is, this light etching process results in contact holes having a cross-sectional shape which falls along a mild curve. Consequently, the coverage of the interconnect electrodes is quite good.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1(A)-1(D) and 2(A)-2(D) are cross-sectional views of a semiconductor device, illustrating a process sequence for fabricating the device by a method according to the present invention;

Fig. 3 is a cross-sectional view of a contact hole formed by the process sequence shown in Figs. 1(A)-1(D) and 2(A)-2(B);

Fig. 4 is a cross-sectional view of a contact hole as shown in Fig. 2 (C) in which corners have been rounded off by a method according to the present invention;

Fig. 5 is a graph illustrating the endpoint of a dry etching process;

Figs. 6(A)-6(C), 7(A)-7(B), and 8(A)-8(B) are cross-sectional views illustrating IC fabrication processes according to the invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS

Embodiment 1

A process sequence for fabricating TFTs in accordance with the present invention is illustrated in Figs. 1(A)-1(D) and Fig. 2(A)-2(D).

First, a glass substrate 101 having an insulating film such as a silicon oxide film on its surface is prepared. An amorphous silicon film (not shown) having a thickness of 500 Å is formed on the substrate by plasma CVD or LP thermal chemical vapor deposition. The amorphous film is crystallized by an appropriate crystallization method, which may be either heating or laser illumination.

Then, the crystalline silicon film obtained by crystallizing the amorphous silicon film is patterned into islands of a semiconductor layer 102 forming an active layer.

A silicon oxide film 103 which will act as a gate-insulating film later is formed on the semiconductor layer to a thickness of 1200 Å by plasma CVD or LP thermal chemical vapor deposition.

Then, a film 104 consisting only or mainly of aluminum is formed to a thickness of 4000 Å. This film 104 will act as a gate electrode later. Of course, other materials capable of being anodized such as tantalum and niobium may also be used.

Thereafter, anodization is carried out within an electrolytic solution, using the aluminum film 104 as an anode. The electrolytic solution is neutralizing 3% ethylene glycol solution of tartaric acid with aqueous ammonia and adjusting it to a pH of 6.92. Using a platinum cathode, the liquid is processed with an electric current of 5 mA. The voltage is increased up to 10 V.

A dense anodic oxide film 105 formed in this way acts to improve the adhesion to photoresist later. The thickness of the anodic oxide film 105 can be controlled by controlling the voltage application time (Fig. 1(A)).

Then the aluminum film 104 is patterned to formed a gate electrode (not shown).

Then, a second anodic oxidation process is carried out to form a

porous anodic oxide film 106. As an electrolytic solution, 3% aqueous solution of oxalic acid is used. A platinum cathode is employed. It is processed with an electric current of 2 to 3 mA. The voltage is increased up to 8 V.

At this time, the anodic oxidation progresses parallel to the substrate. The width of the porous anodic oxide film 106 can be controlled by the voltage application time.

After removing the photoresist with appropriate peeling liquid, a third anodic oxidation process is performed, thus obtaining a state shown in Fig. 1(B).

At this time, the electrolytic solution is neutralizing 3% ethylene glycol solution of tartaric acid with aqueous ammonia and adjusted to a pH of 6.92. Using a platinum cathode, the anodic oxidation is performed with an electric current of 5 to 6 mA. The voltage is increased up to 100 V.

The resulting anodic oxide film 107 is very dense and firm. Therefore, this protects the gate electrode 108 from damage in later steps such as implantation step.

The firm anodic oxide film 107 is not readily etched and so the etching time is prolonged when contact holes are formed. Therefore, it is desired to suppress the thickness of the film below 1000 Å.

Then, a dopant is implanted into the islands of semiconductor layer 102 by the ion implantation process. For example, when an N-channel TFT is manufactured, phosphorus (P) may be used as the dopant.

First, under the condition of Fig. 1(B), a first ion implantation process is carried out. Phosphorus (P) is implanted at an accelerating voltage of 60 to 90 kV at a dose of 0.2 to 5 x 10^{15} atoms/cm^2. In the present example, the accelerating voltage is 80 kV, and the dose is 1 x

10^{15} atoms/cm^2.

Using the gate electrode 108 and the porous anodic oxide film 106 as masks. Regions 109 and 110 which will become source/drain regions are formed by self-aligned technology.

Then, as shown in Fig. 1(C), the porous anodic oxide film 106 is removed, and a second implantation process is performed. The second incorporation of phosphorus (P) is carried out at an accelerating voltage of 60 to 90 kV at a dose of 0.1 to 5 x 10^{14} atoms/cm^2. In the present example, the accelerating voltage is 80 kV, and the dose is 1 x 10^{14} atoms/cm^2.

The gate electrode 108 serves as a mask. Regions 111 and 112 more lightly doped than the source drain 109 and drain region 110 are formed by self-aligned technology.

At the same time, a region 113 acting as a channel for the TFT is formed by self-aligned technology, because no dopant is implanted at all right under the gate electrode 108.

The lightly doped drain (LDD) regions 112 formed in this way suppress generation of a high electric field between the channel region 113 and the drain region 110.

Then,irradiating with KrF excimer laser light and thermally annealing are performed. In the present example, the energy density of the laser light is 250 to 300 mJ/cm^2. The thermal annealing is carried out at 300 to 450°C for 1 hour.

This step can heal the damage to the crystallinity of the islands of semiconductor layer 102 sustained by the ion implantation process.

Then, as shown in Fig. 1(D), two interlayer insulating films 114 and 115 are formed by plasma CVD. In the present example, the interlayer insulating films 114 and 115 are made of silicon nitride films of different composition ratio.

At this time, the composition ratio of the silicon nitride film forming the second interlayer insulating film 115 gives a higher dry etch rate than that of the first interlayer insulating film 114. For example, the film of higher etch rate can be formed by increasing the pressure of the film-forming gas or the growth temperature or by lowering the RF power.

More specifically, where the first and second films are grown at 250°C and 350°C, respectively, the dry etch rate of the second layer is approximately twice as high as the rate of the first layer.

The pressures of the gases for forming the first and second layers, respectively, are set to 0.3 and 0.7 torr, respectively. In this case, the dry etch rate of the second layer is about 1.5 times as high as the rate of the first layer.

This is a requirement which must be satisfied in order that the tilt angle ß of the second interlayer insulating film 115 be smaller than the tilt angle α of the first interlayer insulating film 114 in the shape of the contact hole shown in Fig. 3.

The total thickness of the first and second interlayer insulating films is 1 to 3 times as large as the thickness of the gate electrode 108 to improve the coverage of the interlayer insulating films. Thus, current leaking via the interlayer insulating films is prevented.

Preferably, the thickness of the first interlayer insulating film 114 is less than one third of the total thickness. If the thickness of the first interlayer insulating film is greater than this, the tilt angle α increases, thus resulting in difficulties in a light etching step carried out later.

A resist mask indicated by 201 in Fig. 2(A) is formed, and a contact hole is formed by dry etching techniques. The composition of the etchant gas is so set that $CF_4:O_2 = 40:60$.

The etching ends when a period of 150 seconds passes since the

endpoint has been confirmed. The endpoint is detected as shown in Fig. 5. The signal intensity of nitrogen ions from the first layer is greater, because the first layer is denser than the second layer.

At this time, in the source/drain contact regions 202 and 203, the gate-insulating film 103 acts as a film that stops the dry etching process. In the gate electrode region 204, the anodic oxide film 107 acts as a film that stops the dry etching process.

Since the second interlayer insulating film 115 is higher in etch rate than the first interlayer insulating film 114, tapered sections are formed as shown in Fig. 2(A).

Then, the gate-insulating film 103 at the bottom surface of the contact hole is etched with buffered hydrofluoric acid, thus completing the contact holes in the source/drain regions.

Thereafter, chromium mixed acid solution consisting of mixture of chromic acid, acetic acid, phosphoric acid, and nitric acid is used to etch the anodic oxide film 107, thus completing the contact hole in the gate electrode region.

Where the gate-insulating film 103 is etched first in this way, the gate electrode 108 can be protected, since the anodic oxide film 107 has excellent resistance to buffered hydrofluoric acid. The chromium mixed acid solution hardly attacks the source region 109 or drain region 110.

In this way, the state shown in Fig. 2(B) is obtained. Wet etching using buffered hydrofluoric acid or chromium mixed acid progresses isotropically and so overetched portions as shown in the circles of Fig. 2(B) are formed.

The interlayer insulating films are recessed by light etching, thus eliminating overetched portions, as shown in Fig. 2(C). At this time, as the tilt angle α of the first interlayer insulating film 114 decreases, the film can be more easily recessed.

This light etching process is carried out by dry etching techniques. The composition of the etchant gas is so set that $CF_4:O_2 = 25:75$. With this composition, the selectivity of silicon nitride with respect to silicon is more than 10. Hence, the surfaces of the source region 109 and drain region 110 are hardly etched.

This light etching is carried out by the gas with a high O_2 content. Therefore, the resist mask 201 is recessed simultaneously. Consequently, the corners of the cross-sectional shape at the edges of the contact hole are etched away and rounded off, as shown in the circle of Fig. 4.

After the completion of the contact hole, interconnect electrodes 205, 206, and 207 are formed. Then annealing is performed in a hydrogen ambient at 350°C for 2 hours.

A thin-film transistor as shown in Fig. 2(D) is fabricated by performing the steps described above.

Embodiment 2

The present example is an example of application of the present invention to an IC fabrication process using single-crystal silicon wafer. More specifically, this is an example of fabrication of a MOS transistor, using the silicon wafer.

The process sequence of the present invention is shown in Figs. 6(A)-6(C), 7(A)-7(B), and 8(A)-8(B). First, as shown in Fig. 6(A), a thermal oxide film and a silicon nitride film are laminated over an N-type single-crystal silicon wafer 601 and patterned to create a patterned lamination of the thermal oxide film 602 and silicon nitride film 603.

Then, field oxide films 604 and 605 are formed by a selective thermal oxidization method. Thus, a state shown in Fig. 6(A) is obtained.

Then, the thermal oxide film 602 and the silicon nitride film 603

are removed. A thermal oxide film 606 is formed again by thermal oxidation. This thermal oxide film 606 forms a gate-insulating film.

Thereafter, a gate electrode 607 is fabricated from an appropriate metal material, silicide material, or semiconductor material. Subsequently, dopants are implanted to form source/drain regions.

In this example, boron (B) ions are introduced through ion implantation to fabricate a P-channel MOS transistor. If an N-channel MOS transistor is fabricated, phosphorus (P) ions may be introduced.

After the ion implantation described above, a heat-treatment is made to activate the introduced dopants and to anneal out damage to the semiconductor layer caused by the ion implantation.

In this way, a P-type source region 608 and a drain region 609 are formed by self-aligned technology, as shown in Fig. 6(B).

Then, silicon nitride films 610 and 611 are formed as interlayer insulating films. In the same way as in Example 1, the silicon nitride films 610 and 611 have such film properties that the film 611 has a higher etch rate than the below film 610.

A state shown in Fig. 6(C) is obtained in this manner. Then, as shown in Fig. 7(A), a resist mask 612 is placed. Contact holes 613 and 614 are formed by dry etching techniques.

A state shown in Fig. 7(A) is obtained in this way. At this time, the gate-insulating film 606 consisting of a thermal oxide film acts as an etch stopper.

Contact holes 615 and 616 are then formed by wet etching techniques.

In this manner, a state shown in Fig. 7(B) is obtained. At this time. wet etching proceeds isotropically and so the contact holes 615 and 616 widen the bottoms of the contact holes 613 and 614, respectively.

Then, the interlayer insulating films and resist mask are recessed

by light dry etching, using mixture of CF_4 and O_2. The oxygen is added, because the resist mask should be recessed.

In this way, contacts having a mild cross-sectional shape as shown in Fig. 8(A) can be obtained. After obtaining the state shown in Fig. 8(A), a source electrode 619 and a drain electrode 620 are formed as shown in FIg. 8(B), thus completing a MOS transistor.

In the present invention, the interlayer insulating film is made of a multilayer structure consisting of two or more layers. The etch rate of an upper layer is made higher than that of a lower layer. Therefore, tapered section can be formed in such a way that the tilt angle decreases successively from the top layer of the interlayer insulating film toward the bottom layer.

Furthermore, undercutting of the gate-insulating film 103 and of the anodic oxide film 107 as shown in the circles of Fig. 2(B) can be prevented. In addition, the cross-sectional shape around the top of each contact hole can be improved as shown in Fig. 2(C) and 3.

The cross-sectional shape of the contact hole can be improved greatly by the effects described above. The yield at which TFTs are fabricated and the reliability of interconnect contacts are enhanced. Concomitantly, the long-term reliability of the devices and display system can be enhanced.

What is claimed is:

1. A method of fabricating a thin-film transistor comprising a gate region having a gate electrode made of a material capable of being anodized and source-drain regions made of a semiconductor, said method comprising the steps of:

forming a multilayer insulating film comprising at least two layer over said gate region and over said source-drain regions; and

forming holes in said multilayer insulating film by dry etching techniques so as to form tapered sections having tilt angles which decrease successively from said top insulating layer toward said bottom insulating layer of the film.

ABSTRACT

Method of fabricating thin-film transistors in which contact with connecting electrodes becomes reliable. When contact holes are formed, the bottom insulating layer is subjected to a wet etching process, thus producing undercuttings inside the contact holes. In order to remove the undercuttings, a light etching process is carried out to widen the contact holes. Thus, tapering section are obtained, and the covering of connection wiring is improved.

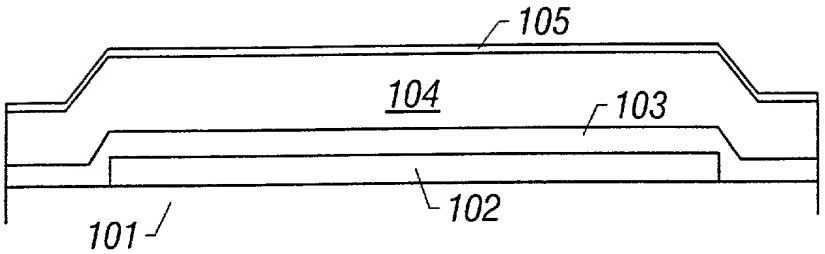

FIG. 1A

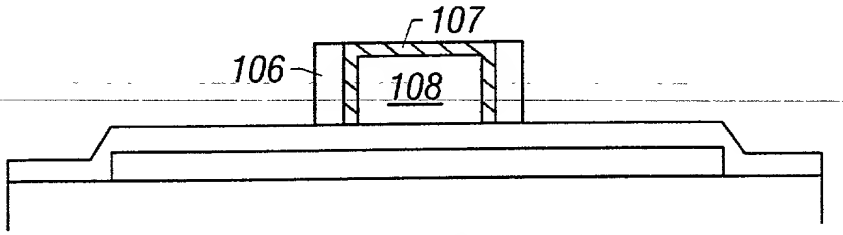

FIG. 1B

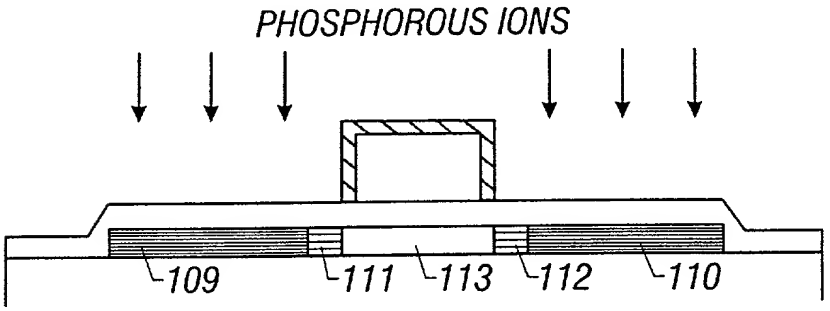

FIG. 1C

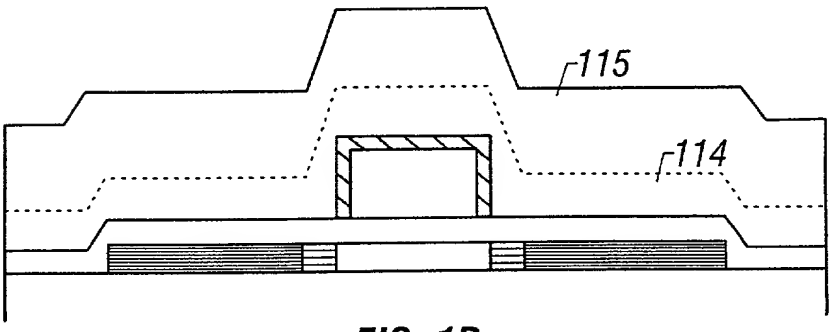

FIG. 1D

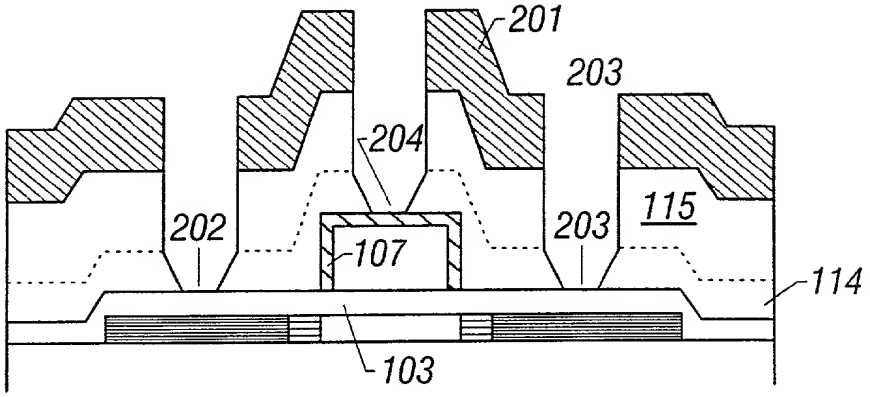

FIG. 2A

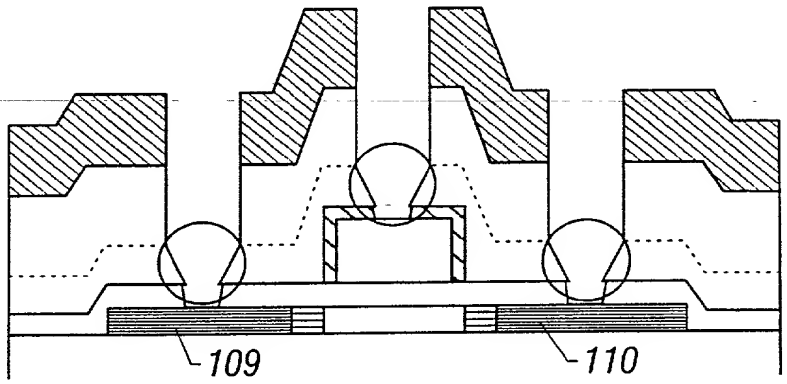

FIG. 2B

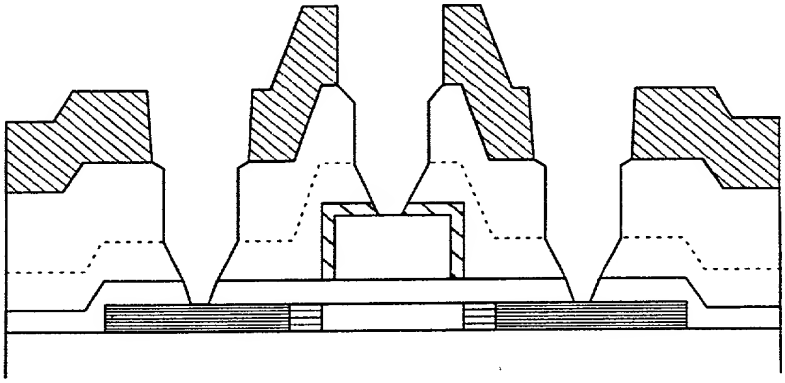

FIG. 2C

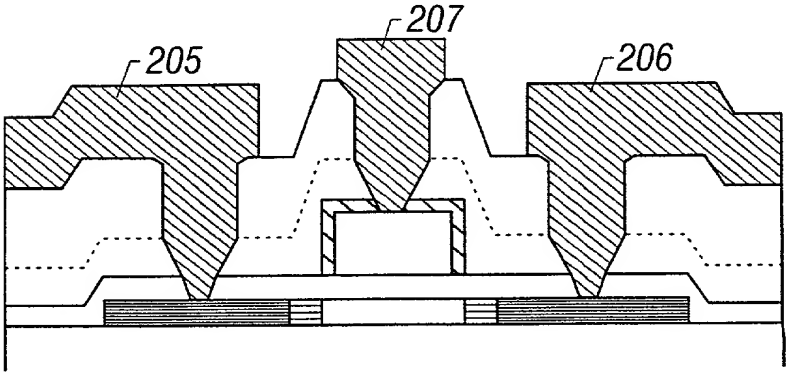

FIG. 2D

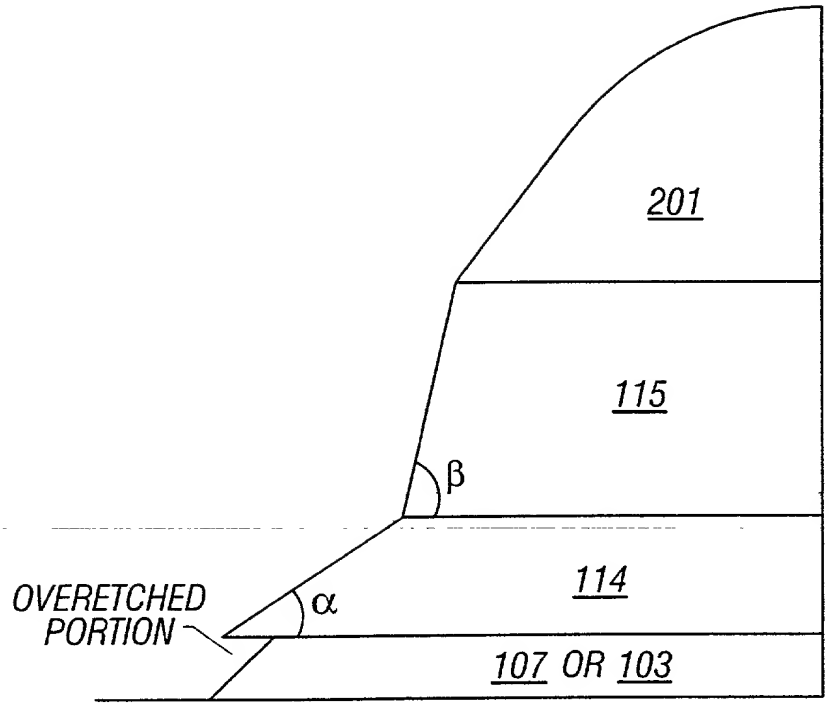
201
115
β
114
OVERETCHED
PORTION
α
107 OR 103

FIG. 3

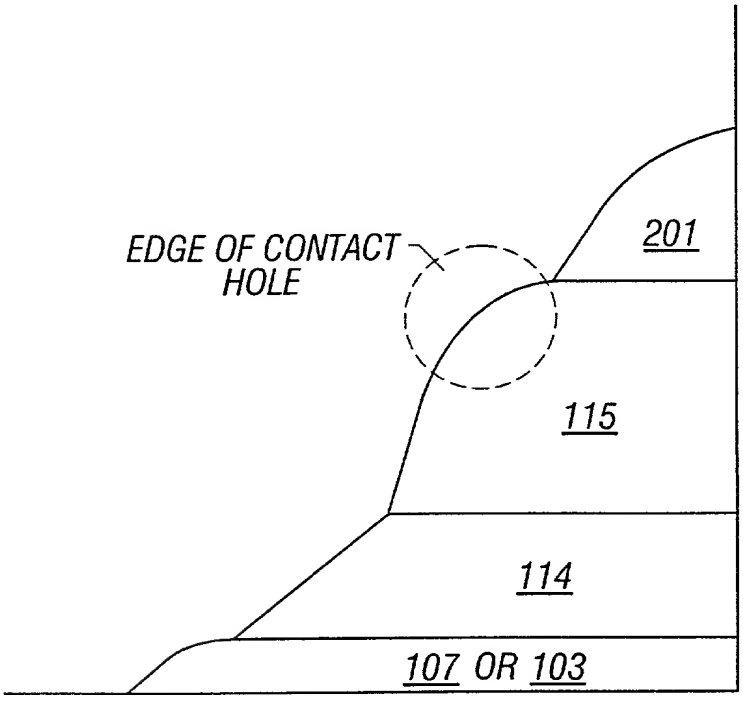
EDGE OF CONTACT
HOLE
201
115
114
107 OR 103

FIG. 4

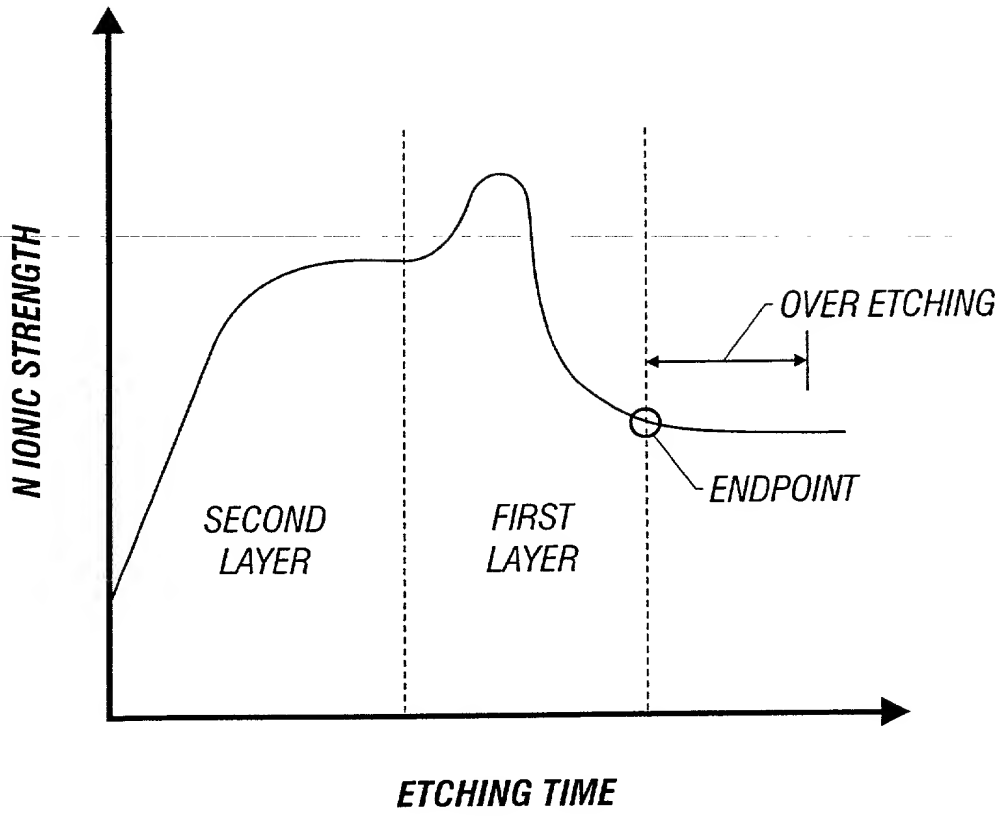
N IONIC STRENGTH
OVER ETCHING
ENDPOINT
SECOND LAYER
FIRST LAYER
ETCHING TIME

FIG. 5

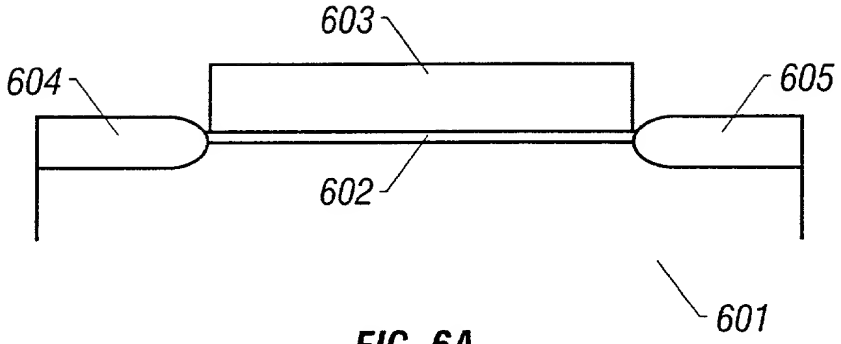

FIG. 6A

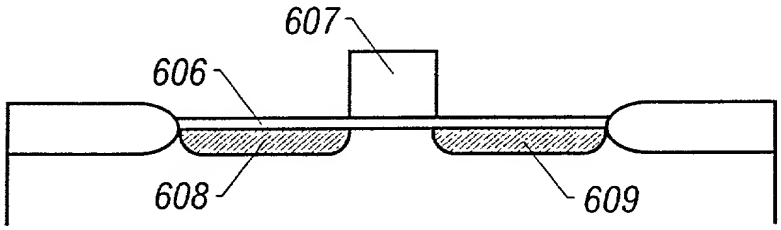

FIG. 6B

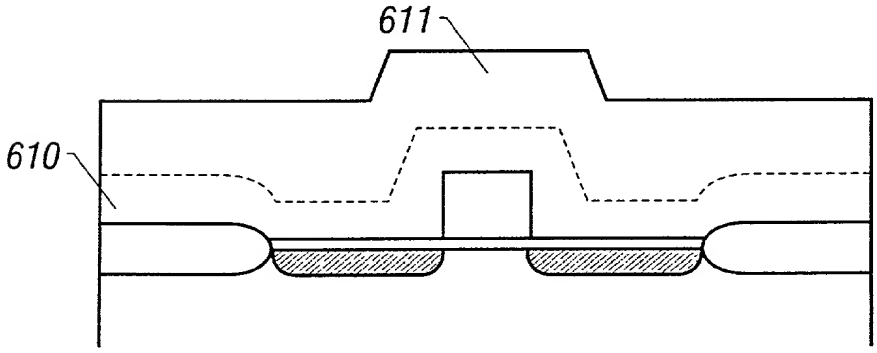

FIG. 6C

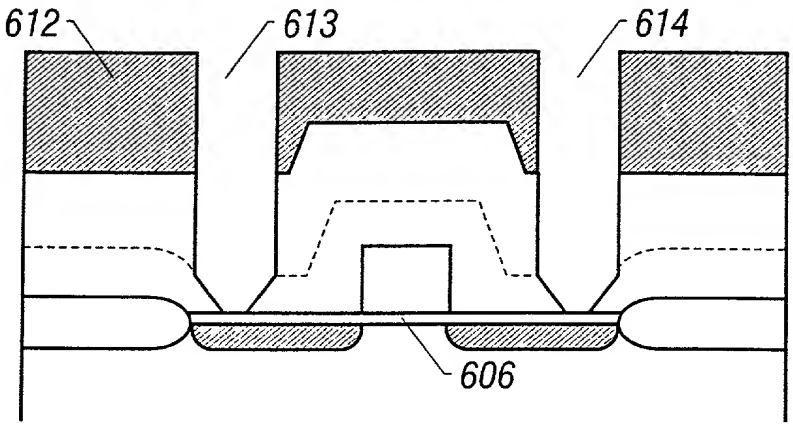

FIG. 7A

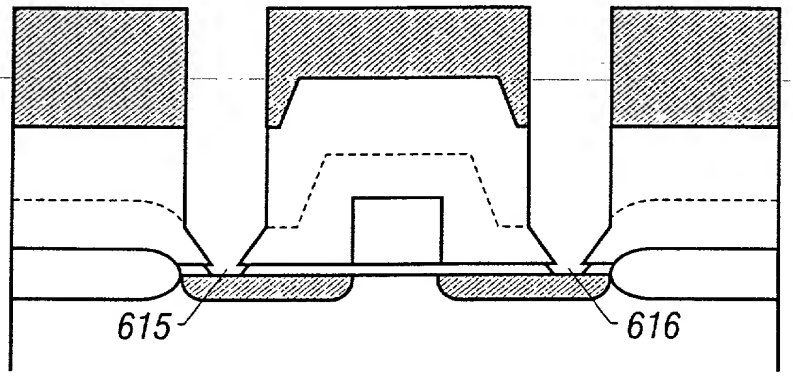

FIG. 7B

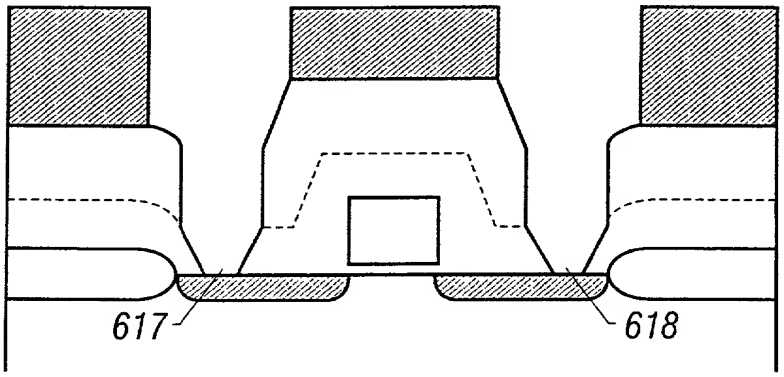

FIG. 8A

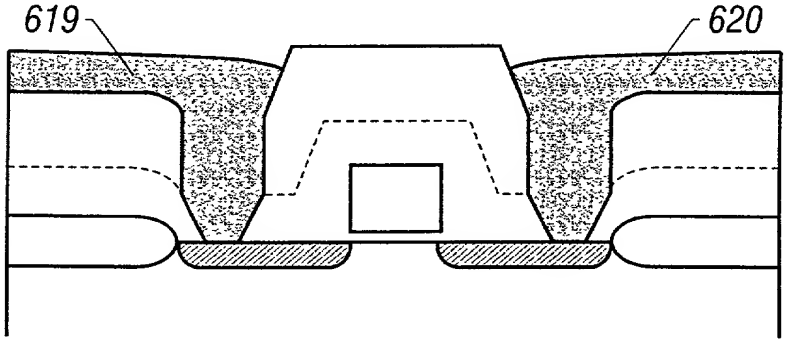

FIG. 8B

PATENT
ATTORNEY DOCKET NO: 07977/ 088001

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHOD OF FABRICATING SEMICONDUCTOR DEVICE

the specification of which

■ is attached hereto.

☐ was filed on _____ as Application Serial No. _____

and was amended on _____.

☐ was described and claimed in PCT International Application No. _____

filed on _____ and as amended under PCT Article 19 on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information I know to be material to patentability in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

COUNTRY	APPLICATION NO.	FILING DATE	PRIORITY CLAIMED
JAPAN	7-332629	November 27, 1995	☒ Yes ■ No
			☐ Yes ■ No
			☐ Yes ■ No
			☐ Yes ■ No

I hereby appoint the following attorneys and/or agents to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: Scott C. Harris Reg. No. 32,030, William E. Booth, Reg. No. 28,933; Barry E. Bretschneider, Reg. No. 28,055; John W. Freeman, Reg. No. 29,066; Timothy A. French, Reg. No. 30,175; Alan H. Gordon, Reg. No. 26,168; John F. Land, Reg. No. 29,554; John B. Pegram, Reg. No. 25,198; Rene D. Tegtmeyer, Reg. No. 33,567; Hans R. Troesch, Reg. No. 36,950; Dorothy P. Whelan, Reg. No. 33,814; Charles C. Winchester, Reg. No. 21,040.

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patents issued thereon.

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Inventor's Signature: Hongyong Zhang Date: November 15, 1996

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Post Office Address: _____

Full Name of Inventor: _____

Inventor's Signature: _____ Date: _____

Residence Address: _____

Citizen of: _____

Post Office Address: _____